

BENEFITS OF SIMULTANEOUS DATA ACQUISITION MODULES

When choosing a data acquisition board, many different selection criteria are used. Speed, resolution, accuracy, and number of channels are all important considerations. In addition, there are different architectures used within the data acquisition device itself that can affect your decision. The particular analog input architecture that you choose will affect how often the input channels are sampled and the accuracy of your results.

The two most common architectures in analog input design are multiplexed and simultaneous. Multiplexed architectures use one A/D converter for many channels. Conversely, simultaneous architectures use an individual A/D converter for each channel.

Simultaneous A/D Architecture

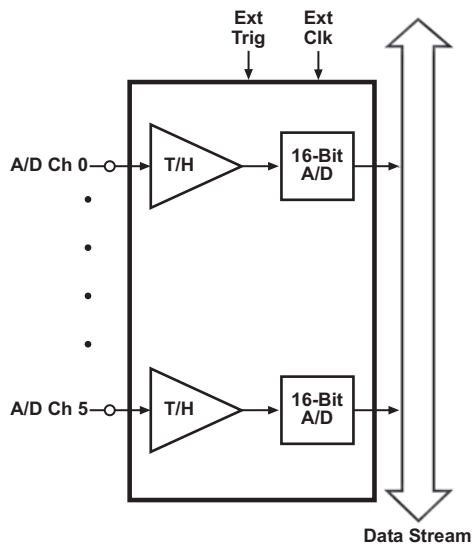


FIGURE 1

Simultaneous Architecture: One A/D converter per channel.

Conventional Multiplexed A/D Architecture

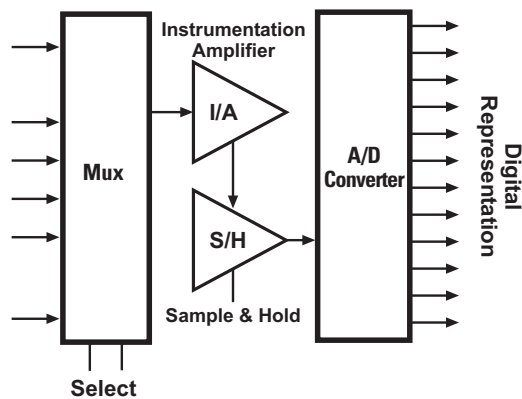


FIGURE 2

Conventional Multiplexed Architecture: Many channels multiplex into one A/D converter.

For many applications, a simultaneous acquisition device is certainly the architecture of choice due to its inherent speed and accuracy but, until recently, the cost of these devices was somewhat prohibitive. Times have changed and simultaneous devices are now as cost effective as a multiplexed device for most users.

Data Translation has designed a series of simultaneous data acquisition modules for USB 2.0. Useful in the following applications, the Simultaneous Series provide, high speed, highly accurate measurements:

- Semiconductor device testing
- Nanotechnology testing
- Drug discovery
- Scientific analysis
- Automotive testing

The Simultaneous Series modules from Data Translation provide a 16-bit A/D converter for each analog channel. This allows the user to correlate ultra high-speed measurements of up to 2MHz at the exact same instant in time. These modules are also designed with 500V galvanic isolation to maximize signal integrity and protect the PC. This series was developed for customers seeking to correlate highly accurate, high-speed measurements while eliminating phase noise from channel-to-channel acquisition.

With this series, a common clock and trigger are used for simultaneous and synchronous sampling of all inputs. This means that all functions of the data acquisition modules (A/D, D/A, DIO, Counter/Timers, and Quadrature Decoders) can be simultaneously triggered internally or externally. The data can then be clocked either internally or externally and streamed synchronously to host memory.

The synchronous operation allows all I/O data to be processed and correlated for all inputs and outputs. This is very valuable in determining the response across a device-under-test (DUT) to stimuli at the same exact instant.

A more detailed discussion of the benefits of simultaneous acquisition versus the multiplexed approach is provided here to help you make your buying decision.



The Simultaneous Series modules offer up to 2.0MHz sampling rates on USB 2.0.

SIGNAL BANDWIDTH INCREASED

Simultaneous acquisition dramatically increases signal bandwidth because each channel uses the full throughput of an individual A/D converter. Compare the following tables for a 150 kHz module in a multiplexed and simultaneous architecture. You can see that the signal bandwidth is consistent across all channels with the simultaneous architecture, while it decreases linearly with each additional channel in the multiplexed architecture.

MULTIPLEXED ARCHITECTURE:

One A/D converter, one instrumentation amplifier and multiplexer results in the following performance:

Number of Channels Acquired	Sample Rate Per Channel	Signal Bandwidth
1	150kHz	75kHz
2	75kHz	37.5Hz
3	50kHz	25kHz
4	37.5kHz	18.75kHz
5	30kHz	15kHz
6	25kHz	12.5kHz

SIMULTANEOUS ARCHITECTURE:

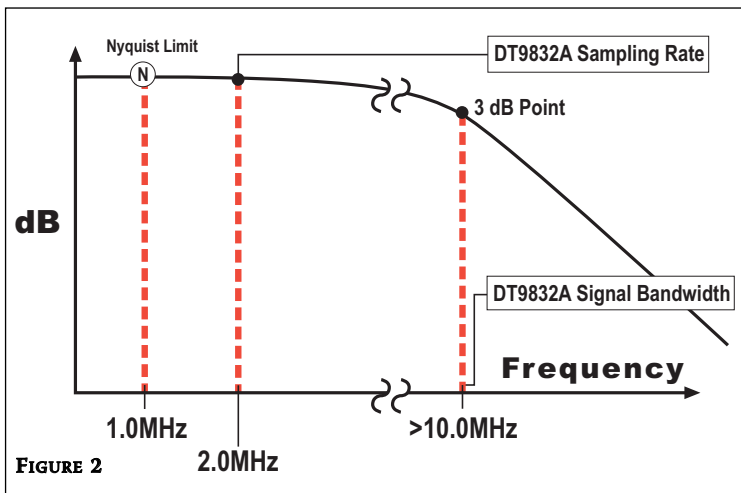
One A/D converter per channel increases the board's overall sampling frequency and increases the signal bandwidth that can be acquired and results in the following performance:

Number of Channels Acquired	Sample Rate Per Channel	Signal Bandwidth
1	150kHz	75kHz
2	150kHz	75kHz
3	150kHz	75kHz
4	150kHz	75kHz
5	150kHz	75kHz
6	150kHz	75kHz

Additionally, the Simultaneous Series from Data Translation is designed to accurately measure higher bandwidth signal components. To accurately measure 16-bit accuracy, the front-end input amplifier has a bandwidth of ten times the Nyquist limit. Below is an example of these design characteristics for the DT9832A.

DT9832A

The DT9832A has a sampling rate for each channel of 2.0 MHz. This means that the Nyquist limit allows signal frequencies up to 1.0 MHz to be adequately measured. The analog input components have a signal bandwidth that is ten times the Nyquist limit or in this case, greater than 10.0 MHz to minimize roll-off and phase errors.



CHANNEL TO CHANNEL SKEW ELIMINATED

As you can see from the figures below, since multiplexed devices use one common amplifier and A/D converter to sample all the input channels being used, a resulting time delay or skew exists between samples. This phase noise is all but eliminated when using a single A/D converter per channel as does the Simultaneous Series modules.

Simultaneous Sampling

eliminates time skew between channels and simplifies both time and frequency based analysis techniques.

Sequentially (Multiplexed) Sampling

may require software correction for detecting certain patterns.

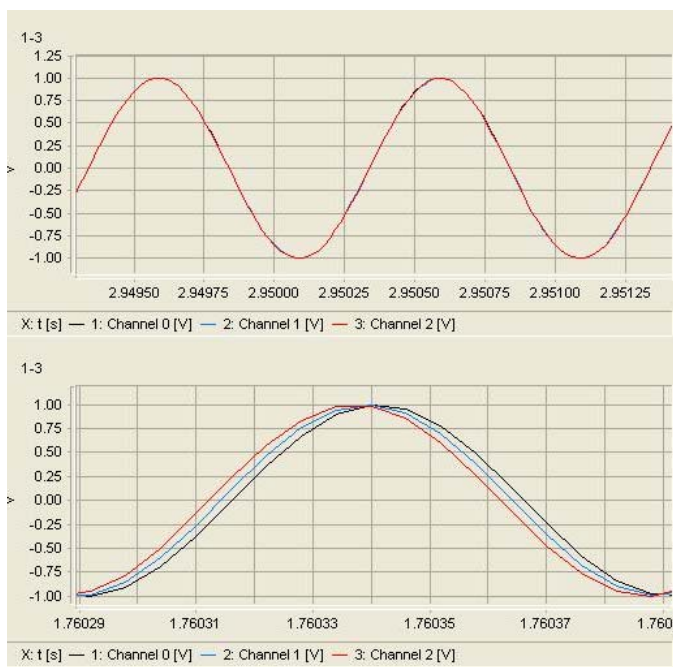
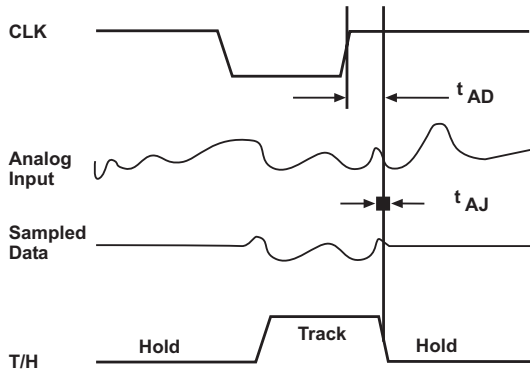


FIGURE 3

BUILT IN ACCURACY

With a simultaneous A/D converter, all signal inputs are sampled at the exact same instant in time. A common clock and trigger for all channels lets you accurately correlate signals using a single pulse of the clock to acquire all channels. The hardware architecture has accuracy built in. A maximum aperture delay of 35ns (the times it takes the A/D on the module to switch from track to hold mode) is well matched at 5ns across all six track-and-hold circuits, virtually eliminating the channel-to-channel skew that is associated with multiplexed inputs. A maximum aperture uncertainty of 1ns (the "jitter", or variance in aperture delay) virtually eliminates time skew between channels and simplifies both time and frequency- based analysis techniques.



t_{AD} = Aperture Delay of 35 ns
 t_{AJ} = Aperture Jitter (Uncertainty) of 1 ns
 The time between each channel (Aperture Delay Matching) is 5 ns maximum.

FIGURE 4

The A/D design of simultaneous modules features built-in accuracy. A maximum aperture delay of 35 ns (the time it takes the A/D to switch from track to hold mode) is well matched at 5 ns across all track-and-hold circuits, virtually eliminating channel-to-channel skew that is associated with multiplexed inputs. A maximum aperture uncertainty of 1 ns (the jitter or variance in aperture delay) virtually eliminates phase noise in your data.

HIGHER ACCURACY AT HIGH SPEED

Simultaneous A/Ds are far more accurate than multiplexed A/Ds, especially at high speed, because they eliminate several sources of error, including settling time, and channel-to-channel crosstalk, explained below.

SETTLING TIME

Not only is the channel-to-channel skew virtually eliminated with the simultaneous A/D architecture, but so is the time needed to discharge the built-up capacitance on each input of a multiplexed A/D.

Multiplexed

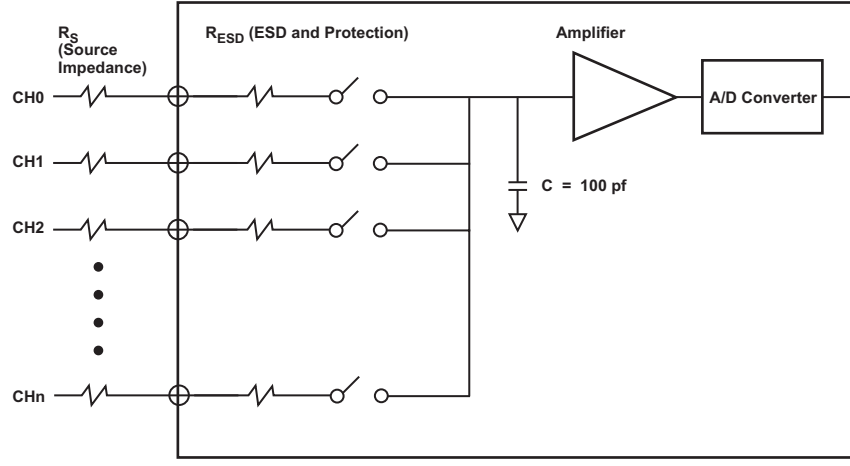


FIGURE 5

Simultaneous

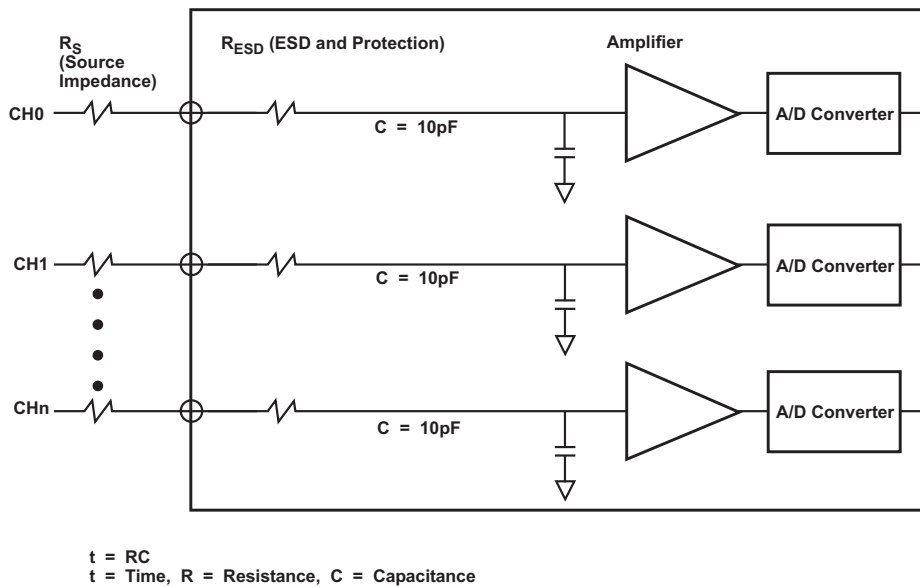


FIGURE 6

Figure 5 and 6 show an equivalent RC circuit for a multiplexed A/D versus a simultaneous A/D. As you can see, in a multiplexed architecture, each channel is tied to the same A/D. A minimum settling time is required for the switched voltage to reach the actual input signal level. If you do not factor the settling time into your sampling rate, some portion of the signal from the previous channel can "cross over" to the next channel (especially when using high source impedance), and generate erroneous results. This effect is most serious when the signal on the previous channel is much larger than the signal on the present channel, and when you try to sample at high speeds.

Because simultaneous architectures have a separate A/D for each input, settling time between channels is not an issue. That means you can acquire data at very high speeds virtually error-free!

SOURCE IMPEDANCE AND SETTLING TIME

Let's look at the multiplexed A/D a little closer. Source impedance (Rs) and capacitance (C), when multiplied together, determine one time constant (t).

The Effect of Input Impedance on Settling Time for Multiplexed A/Ds

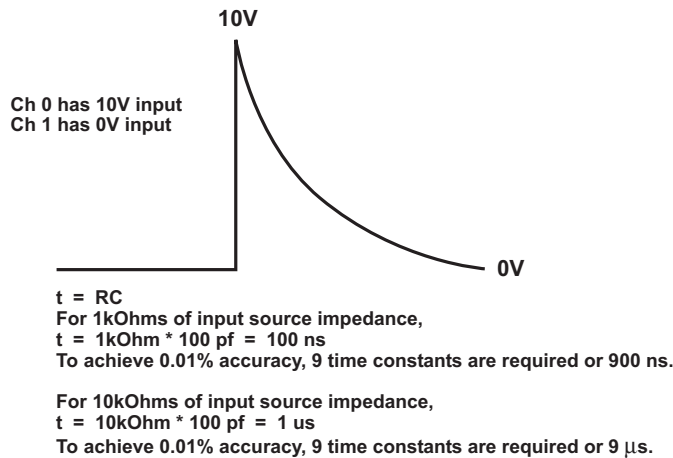


FIGURE 7

Assume that you have a 10 V input on channel 0 and a 0 V input on channel 1. Also assume that the input impedance on channel 1 is 1 kOhm ($R_s = 1 \text{ kOhm}$). Since it typically takes 9 time constants for the multiplexer to settle to within 0.01% accuracy of the voltage you want, the time that it takes to settle when switching from 10 V on channel 0 to 0 V on channel 1 is $9 * 100 \text{ ns}$ ($1\text{kOhm} * 100\text{pf}$), or 900 ns.

Now, assume that you have a source impedance of 10 kOhm ($R_s = 10 \text{ kOhm}$) on channel 1. If the capacitance is 100 pf, the settling time for one channel is $9 * 1 \text{ us}$ ($10\text{kOhm} * 100\text{pf}$) or 9 us - a large source of error if you're sampling too fast!

Simultaneous A/Ds eliminate switching between inputs and, therefore, eliminate the settling time problems associated with high source impedance, allowing you to measure highly accurate data at high speeds.

CHANNEL-TO-CHANNEL CROSSTALK

Another problem with multiplexed systems which is eliminated with simultaneous A/Ds is channel-to-channel crosstalk. Crosstalk occurs when the signals on one or more multiplexed channels couple, or interfere, with the signal on the channel that is being measured. Crosstalk is inherent to the multiplexing process, and gets worse as you increase the channel count and/or the signal frequency.

Crosstalk occurs because parasitic capacitance across each open switch couples a portion of each channel signal going to the output, distorting the desired signal. Figure 8 shows an example of channel crosstalk, where the 5 pf capacitor can cause crosstalk between channels. In this

Cross Channel Talk

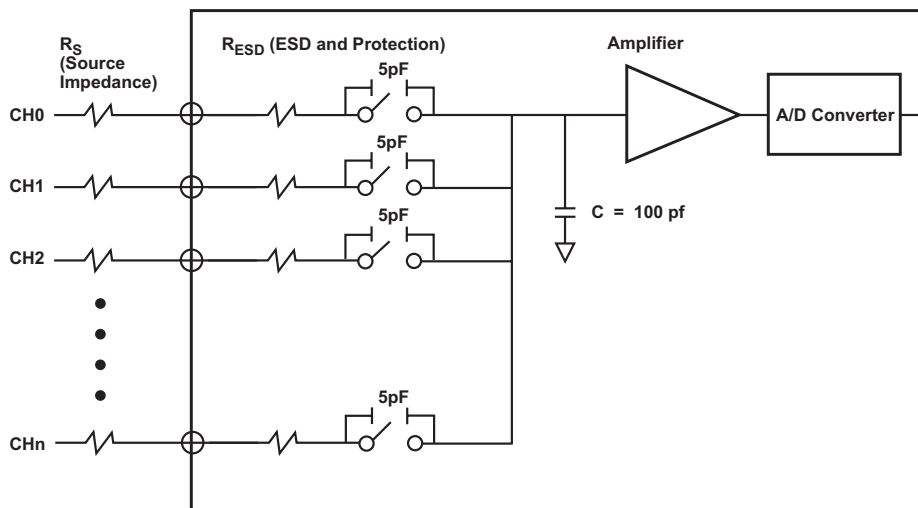


FIGURE 8

example, if the switch for one channel is on and the switches for the other 15 channels are off, the crosstalk is 75 pf (5 pf x 15 channels).

ADDING OP AMPS TO YOUR SIGNAL CONDITIONING

If you are using a multiplexed A/D, you also need to be aware of problems that can occur when adding operational amplifiers (op amps) to your signal conditioning circuitry. Slow-speed op amps have long settling times, which as described previously, can introduce errors into your

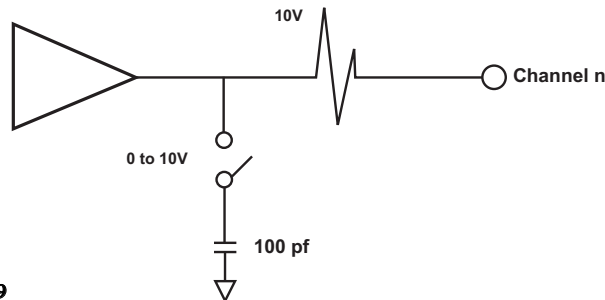


FIGURE 9

measurement. High-speed op amps, on the other hand, will ring when they are hit with the switch transients (100 pf capacitor) from the multiplexer because it takes time for the voltage to settle, as shown in Figure 9.

LESS APERTURE JITTER

Aperture jitter (uncertainty) can be measured by simultaneously inputting a +/- 10 volt sinusoidal signal at a specified frequency across all A/D channels. The sampled data is then analyzed to characterize the A/D converter's ability to sample all channels at precisely the same moment.

Since a sinusoidal signal's rate-of-change is greatest at the zero-crossings (locations on the signal where negative-to-positive voltage transitions occur), aperture jitter is most effectively measured there.

A sinusoid is determined by the following equation:

$$V(t) = p \sin(2\pi ft)$$

where,

p = peak voltage of sine wave

f = frequency of sine wave

V = voltage

t = time (in seconds)

$$\frac{dV}{dt} = 2\pi fp$$

In order to find the voltage change near the zero-crossing, take the derivative of the above equation evaluated at $t = 0$.

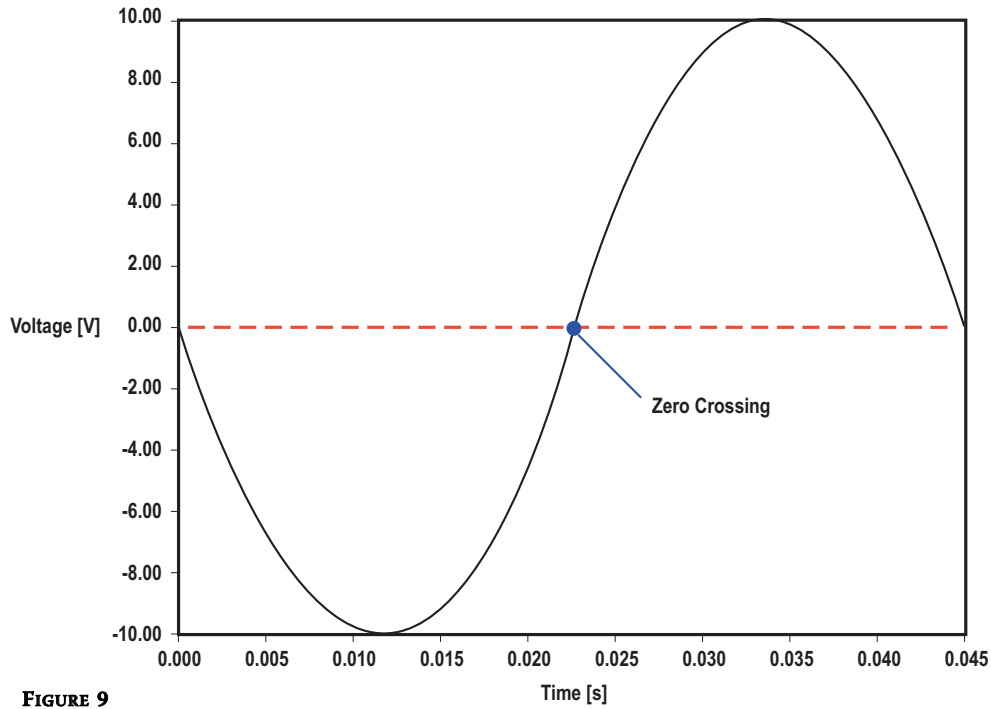


FIGURE 9

Aperture jitter is most effectively measured where the signals rate of change is greatest, which is the zero crossing as illustrated above.

APERTURE JITTER (UNCERTAINTY)

Aperture Jitter (ns)	Peak Voltage	Frequency (Hz)	12-Bit A/D Error (Number of Lsb's)	16-Bit A/D Error (Number of Lsb's)
1	10	100	.001	.021
1	10	1000	.013	.206
1	10	10000	.13	2.06

Using this equation with an aperture uncertainty of 1 ns, a 10 kHz signal should yield a voltage change near the origin of 628 μ V or \sim 2 bits of error for a 16-bit A/D converter.

Data Translation offers a full line of simultaneous acquisition boards for USB 2.0.

These products include:

DT9836 & DT9832 Series - Simultaneous, high performance, isolated analog inputs provide throughput rates up to of 2.0MHz per channel. Analog outputs, digital I/O, quadrature decoders, and counter/timers included.



DT9816 & DT9816-A - Low Cost Simultaneous A/D Module. Part of the ECONseries of low-cost, multi-function, non-isolated USB modules.



DT9840 Series – Real-time simultaneous A/D and D/A DSP multi-function USB module enclosed in a Sleek Box. Uses the Texas Instruments TMS320C6713 DSP chip.

